WHAT IS CLAIMED IS:

1. A group-III nitride semiconductor stack, comprising:

a single-crystal substrate;

a first group-III nitride layer formed on a principal surface of the single-crystal substrate;

a graded low-temperature deposited layer formed on the group-III nitride layer and made of nitride in which group-III element composition is continuously changed; and

a second group-III nitride layer formed on the graded low-temperature deposited layer.

2. The group-III nitride semiconductor stack according to claim 1, wherein the graded low-temperature deposited layer is continuous with the first and second group-III nitride layers in terms of composition and represented by a compositional formula AlxGa1-xN in which a composition ratio x changes between 0 and 1.

3. The group III nitride semiconductor stack according to claim 2, wherein in the compositional formula AlxGa1-xN, the composition ratio x increases from 0, becomes a maximum at a center portion of the graded low-temperature deposited layer, decreases again, and becomes 0 at an uppermost portion of the graded low-temperature deposited layer along a direction of growth of films on the first group-III nitride layer.

4. The group-III nitride semiconductor stack according to claim 3, wherein the composition ratio x becomes 1 at the center portion of the graded low-temperature deposited layer.

5. The group-III nitride semiconductor stack according to claim 1, wherein the first group-III nitride layer is an undoped GaN layer, and the second group III nitride layer is a Si doped n-type GaN layer.

6. The group-III nitride semiconductor stack according to claim 1, wherein the number of the graded low-temperature deposited layers formed is more than 1.

7. The group-III nitride semiconductor stack according to claim 6, wherein the plurality of graded low-temperature deposited layers are first and second graded low-temperature deposited layers, the second graded low-temperature deposited layer being continuously placed directly on the first graded low-temperature deposited layer.

8. The group-III nitride semiconductor stack according to claim 6, wherein the plurality of graded low-temperature deposited layers are first and second graded low-temperature deposited layers, the second graded low-temperature deposited layer being placed on a GaN layer grown at high temperature directly on the first graded low-temperature deposited layer, the GaN layer being any one of an n-type GaN layer and an undoped GaN layer.

9. A method of manufacturing a group-III nitride semiconductor stack, comprising:

forming a first group III nitride layer on a principal surface of a single-crystal substrate;

forming a graded low-temperature deposited layer in which

group-III element composition is continuously changed, on the first group-III nitride layer without growth interruption; and

forming a second group-III nitride layer on the graded low-temperature deposited layer without growth interruption.

10. The method according to claim 9, wherein the graded low-temperature deposited layer is continuous with the first and second group-III nitride layers in terms of composition and represented by a compositional formula AlxGa1-xN in which a composition ratio x changes between 0 and 1.

11. The method according to claim 9, wherein the first group-III nitride layer is an undoped GaN layer and the second group-III nitride layer is a Si-doped n-type GaN layer.

12. The method according to claim 9, wherein the graded low-temperature deposited layer is formed by continuously supplying raw material without interruption, being performed controlled continuous temperature lowering and continuous temperature raising, and starting with a growth temperature for the first group-III nitride layer.

13. The method according to claim 12, wherein the temperature lowering is performed in a temperature range of a growth temperature for the first group-III nitride layer to a lowest growth temperature between 500 °C and 650 °C, and the temperature raising is performed in a temperature range of the lowest growth temperature to a growth temperature for the second group-III nitride layer.

14. The method according to claim 9, wherein the graded

low-temperature deposited layer is formed by continuously supplying raw material without interruption, being performed controlled continuous temperature lowering, and starting with a growth temperature for the first group-III nitride layer.

15. The method according to claim 14, wherein the temperature lowering is performed in a temperature range of the growth temperature for the first group-III nitride layer to a lowest growth temperature between 500 °C and 650 °C.

16. A group-III nitride semiconductor device, comprising:

a single crystal substrate;

an undoped group-III nitride layer formed on a principal surface of the single crystal substrate;

a graded low-temperature deposited layer which is formed on the undoped group-III nitride layer and in which group-III element composition is continuously changed;

an n-type group-III nitride contact/cladding layer formed on the graded low-temperature deposited layer;

a group-III nitride MQW active layer formed on the n-type group-III nitride contact/cladding layer;

a p-type group-III nitride cladding layer formed on the group-III nitride MQW active layer; and

a p-type group-III nitride contact layer formed on the p-type group-III nitride cladding layer.

17. The group-III nitride semiconductor device according to claim 16, wherein the undoped group-III nitride layer is a GaN layer, the graded low-temperature deposited layer is AlxGa1-xN

in which a composition ratio x changes between 0 and 1, and the n-type group-III nitride contact/cladding layer is a Si-doped GaN layer.

18. The group-III nitride semiconductor device according to claim 17, wherein in the compositional formula AlxGa1-xN, the composition ratio x increases from 0, becomes a maximum at a center portion of the graded low-temperature deposited layer, decreases again, and becomes 0 at an uppermost portion of the graded low-temperature deposited layer along a direction of growth of films on the first group-III nitride layer.

19. The group-III nitride semiconductor device according to claim 18, wherein the composition ratio x becomes 1 at the center portion of the graded low-temperature deposited layer.

20. The group-III nitride semiconductor device according to claim 16, wherein the number of the graded low-temperature deposited layers formed is more than 1.